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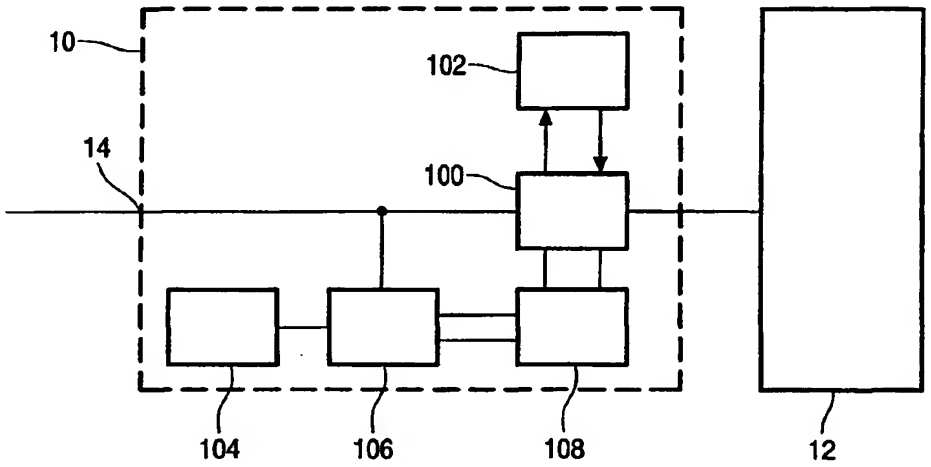
(54) Title: DATA PROCESSING APPARATUS THAT IDENTIFIES A COMMUNICATION CLOCK FREQUENCY



(57) Abstract: A data processing apparatus receives a message containing a sync break interval with a unique bit pattern and a sync field interval identified by the sync break interval. A timing property of the sync field interval specifies the length of bit periods of the message. A clock source circuit supplies a sampling clock signal to define time points for sampling bits from the message. The clock source circuit adapts a frequency of the sampling clock signal to the timing property of the sync field interval. The clock source circuit searches for potential sync break intervals that match the unique bit pattern for a range of bit period values and verifies for each potential sync break interval whether the sync field interval identified by that potential sync break interval specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period, as a condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval identified by the potential sync break interval. Supply of sampling clock signals is preferably suppressed after an end of a preceding message until said condition is met.

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